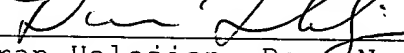


REMARKS

The claims have been amended to delete multiple dependencies. The above amendments are submitted to place this application in proper U.S. format. Entry of the amendment and an early action on the merits are solicited.

Respectfully submitted,

By   
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## Appendix A

### Version with Markings to Show Changes Made to the Claims

The following are marked up versions of amended claims 3, 4, 5, 6, 7 and 8:

- 1 3. (Amended) AGC circuit according to claim 1 ~~or 2~~,  
2 characterized in that the threshold circuit comprises first and  
3 second comparators for comparing the output signal of the level  
4 detector with positive and negative threshold levels around a zero  
5 level for initiating the digital gain control signal generator for  
6 a stepwise variation of the gain of the digitally controlled  
7 amplifier.
- 1 4. (Amended) AGC circuit according to claim 1 ~~one of claims 1 to~~  
2 ~~3~~, characterized in that the digital gain control signal generator  
3 comprises a pulse generator coupled to a clock-signal input of a  
4 digital counter for supplying a clock-signal thereto, the threshold  
5 circuit including a third comparator for comparing the output  
6 signal of the level detector with a zero level, an output of the  
7 third comparator being coupled to an up/down input of the counter.
- 1 5. (Amended) AGC circuit according to claim 3 ~~one of claims 3 or~~  
2 ~~4~~, characterized in that the gain variation range of the  
3 continuously controlled amplifier caused defined by the range of  
4 the continuous gain control signal between the negative and  
5 positive threshold levels, corresponds at least to the gain  
6 variation of the digitally controlled amplifier over two  
7 consecutive incremental steps of said digital gain control signal.

1 6. (Amended) AGC circuit according to claim 4 ~~one of claims 4 to~~  
2 5, characterized in that the time period between two consecutive  
3 clock pulses of the clock-signal is chosen sufficiently large to  
4 prevent superposition of subsequent gain step variations of the  
5 digitally controlled amplifier from occurring.

1 7. (Amended) AGC circuit according to claim 1 ~~one of claims 1 to~~  
2 6, characterized in that the time-constant of the loop-filter is  
3 chosen sufficiently large to prevent regenerative feedback of the  
4 gain control signal in the AGC loop from occurring.

1 8. (Amended) Receiver for digitally modulated signals comprising  
2 an AGC circuit as claimed in claim 1 ~~one of claims 1 to 7~~,  
3 characterized by said digitally controlled amplifier being coupled  
4 between an RF input filter and a phase quadrature mixer stage,  
5 phase quadrature outputs thereof being coupled through frequency  
6 selective means to a pair of phase quadrature continuously  
7 controlled amplifiers, this pair of phase quadrature continuously  
8 controlled amplifiers being coupled through to a pair of phase  
9 quadrature analogue to digital converters to said level detector.